ABSTRACT OF THE DISCLOSURE

A parallel signal automatic phase adjusting circuit includes a signal generator for generating a signal having a predetermined frequency, an oscillating circuit for generating a clock signal having a frequency smaller than an inputted clock signal by the predetermined frequency, and adjusting circuits, respectively corresponding data signal channels, each adjusting the generated clock signal so as to be synchronized with the corresponding data signal, based on an arithmetic operation of trigonometric functions using both phase comparing information, derived from comparison between the corresponding data signal and the generated clock signal, and frequency information regarding the corresponding data signal, the generated clock signal and the signal from the signal generator. The circuit is useful, for example, when digital data transmitted through a large number of parallel data signal lines between data terminals, because the size of and the cost for the circuit are reduced.